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SUPPLEMENTAL REISSUE DECLARATION

To The Honorable Commissioner of Patents and Trademarks:

Sir:

The undersigned are applicants of the Reissue Application Serial No. 07/985,141, filed December 3, 1992 for Reissue of Letters of Patent for GRAPHIC PROCESSING APPARATUS UTILIZING IMPROVED DATA TRANSFER TO REDUCE MEMORY SIZE, United States Patent No. 4,975,857, granted to them December 4, 1990, of which Hitachi Limited, whose post office address is Tokyo, Japan, is now sole owner by Assignment recorded on April 5, 1989 at Reel 5061 and Frame 277, and on whose behalf and with whose assent the Reissue application is made, hereby reaffirm their offer to surrender said Letters Patent. However, said Letters Patent apparently has been lost. A Declaration under 37 CFR §1.178 stating that said Letters Patent has not been found was filed on March 23, 1994.

The undersigned also reaffirm their appointment of the following attorneys as principal attorneys in this application:

Donald R. Antonelli, Reg. No. 20,296;
David T. Terry, Reg. No. 20,178;
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Carl I. Brundidge, Reg. No. 29,621.

Please direct all communications to the following address:

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We, Koyo KATSURA, Shinichi KOJIMA and Noriyuki KURAKAMI, declare that:

We are subjects of Japan residing respectively at Hitachiota-shi; Maebashi-shi and Takasaki-shi, all of Japan;

We verily believe ourselves to be the original first and joint inventors of the invention described and claimed in the United States Letters Patent No. 4,975,857, and in the specification of the Reissue Application for which invention we solicit a Reissue patent;

We do not know and do not believe that said invention was ever known or used in the United States of America before our invention thereof;

We hereby state that we have reviewed and understand the contents of the specification of the Reissue Application, including the claims, the Declaration under 37 CFR §1.178 filed March 23, 1994 and the Amendment filed in response to the March 9, 1994 Office Action;

We acknowledge the duty to disclose information which is material to the examination of the Reissue Application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a);

We verily believe that the original patent to be wholly or partly inoperative or invalid by claiming less then we had a right to claim in the patent;

Specifically, during review of the specification and claims of U.S. Patent No. 4,975,857, subsequent to its issuance, undertaken as a result of discussions with another party concerning the technology of that party, it was found that the claims thereof were unduly limited in that they called for limitations not necessary to the patentable invention as disclosed.

More particularly it was discovered that an error arose during the prosecution of U.S. application Serial No. 302,332 filed January 27, 1989 from which U.S. Patent NO. 4,975,857 issued due to the failure of the inventors and that of the Japanese Agent and U.S. Attorneys to fully appreciate and recognize that the invention could have been claimed more broadly. Specifically, the error occurred due to the fact that the claims could have been broadened to more simply recite that the invention provides a first bus having M lines interconnecting a memory and a memory controller and a second bus having N lines interconnecting data processor and the memory controller, wherein N and M are integers and N is greater than M, and that the memory controller transfers M bits of data to and from the memory in a time shared fashion and transfers N bits of data in parallel to and from the data processor.

At meetings held in the United States of America on the dates of November 16 through November 20, 1992 with our U.S. Patent Attorneys, the claims of U.S. Patent No. 4,975,857 were studied in more detail and a new set of claims 9-43 were drafted at that time broadening the scope of the claimed invention to

correct the above-described error. These claims were presented in Reissue Application Serial No. 985,141.

Regarding the new claims 9-43, claim 9 is directed to a graphic processing apparatus including memory means for storing graphic data, data processing means for processing the graphic data, memory control means for controlling the transfer of graphic data to the data processing means, a first bus interconnecting the memory means and the memory control means to transfer M bits of data in parallel therebetween and a second bus interconnecting the data processing means and the memory control means to transfer in bits of data in parallel therebetween. In the graphic processing apparatus due to the difference in capacity between the first bus and the second bus a storage means is provided in the memory control means for temporarily storing graphic data sequentially read out via the first bus in a time shared fashion form the memory means. The memory control means transfers the temporarily stored graphic data in parallel to the data processing means via the second bus.

Claim 10 is similar to claim 9 except that the memory control means includes multiplexing means for multiplexing graphic data received in parallel via the second bus from the data processing means. Also the memory control means of claim 10 transfers multiplexed graphic data sequentially in a time shared fashion to the memory means via the first bus.

Claim 11 recites a graphic processing apparatus including memory means having M bit terminals for storing graphic data wherein the graphic data is read out sequentially in a time

shared fashion, and data processing means having N bit terminals for processing graphic data read from the memory means. N is greater than M. Interface means is provided having M bit terminals coupled to the memory means and N bit terminals coupled to the data processing means for transferring graphic data from the memory means to the data processing means. The interface means of the graphic processing apparatus of claim 11 includes converting means for converting sequential graphic data from the M bit terminals of the memory means into parallel graphic data to be supplied to the N bit terminals of the data processing means.

Claim 12 is similar to claim 11 except that the memory means has graphic data written sequentially thereto in a time shared fashion.

Claim 13 is similar to claim 9 except that the memory control means includes converting means for converting M bits of data sequentially read out in a time shared fashion from the memory means via the first bus into N bits of data to be supplied in parallel to the data processing means via the second bus and for converting N bits of data received in parallel from the data processing means via the second bus into M bits of data to be written sequentially to the memory means via the first bus in a time shared fashion.

Claim 14 depends from claim 13 and recites that the segmented M bits of data to be converted are sequentially read out of the memory means in a time shared fashion plural times within a predetermined unit of time based on an address specified by the data processing means.

Claim 15 depends from claim 14 and recites that the N bits of data converted from the M bits of data sequentially read out from the memory means is applied to the data processing means in a unit of time more than two times the predetermined unit of time.

Claim 16 depends from claim 13 and recites that the N bits of data each include an M bit portion of the N bits of data.

Claim 17 provides a data processing apparatus including data processing means for executing data processing, and memory means for storing data which is read out sequentially in a time shared fashion. Interface means is provided having M bit terminals coupled to the memory means and N bit terminals coupled to the data processing means. The interface means controls the transfer of data between the memory means and the data processing means where N is greater than M. A bus having M lines interconnects the memory means and the interface means through the M bit terminals to transfer M bits of data in parallel therebetween. The interface means of the data processing apparatus of claim 17 includes converting means for converting sequential M bits of data from the memory means into N bits of parallel data to be supplied to the data processing means and for converting N bits of parallel data from the data processing means into sequential M bits of data to be written into the memory means.

Claim 18 depends from claim 17 and recites that the sequential M bits of data to be converted is sequentially read out of the memory means in a time shared fashion plural times

within a predetermined unit of time based on the address specified by the data processing means.

Claim 19 depends from claim 18 and recites that the N bits of data converted from the M bits of data sequentially read out from the memory means is applied to the data processing means in a unit of time more than two times the predetermined unit of time.

Claim 20 depends from claim 17 and recites that the M bits of data includes an M bit portion of the N bits of data.

Claim 21 is directed to a memory read method for reading data from a memory in accordance with a request from a processor. The method includes the steps of reading out M bits of data sequentially from the memory through an M bit bus in a time shared fashion for each of M bits based on an address specified by the processor where M is an integer, converting the read out M bits of data into N bits of parallel data where N is an integer and N is greater than M and applying the converted N bits of data to the processor through an N bit bus.

Claim 22 is similar to claim 21 except that claim 22 is directed to a memory write method for writing data generated in a processor in accordance with a request from the processor.

Claim 23 is directed to a memory controller for controlling transference of data between a memory and a processor where an M bit terminals are coupled to the memory, and N bit terminals are coupled to the processor. Converting means is provided between the N bit terminals and the M bit terminals for converting N bits of data into M bits of data. Claim 24 depends from claim 23 and

recites that the M bits of data is sequentially read out of the memory in time shared fashion plural times within a predetermined unit of time. Claim 25 depends from claim 24 and recites that the N bits of data is applied to the processor in a unit of time more than two times the predetermined unit of time.

Claim 26 depends from claim 24 and recites that the M bits of data includes a M bit portion of the N bits of data. Claim 27 depends from claim 23 and recites that the converting means includes storage means for temporarily storing data.

Claim 28 is directed to a memory read method for reading data from a memory in accordance with a request from a processor wherein the data is read out from the memory sequentially in a time shared fashion plural times within a predetermined unit of time. The data read out is converted into parallel data and the parallel data is applied to the processor in a unit of time more than two times the predetermined unit of time. Claim 29 depends from claim 28 and recites that the sequentially read out data forms a portion of the parallel data to be applied to the processor. Claim 30 depends from claim 28 and recites that the data sequentially read out from the memory is composed of M bits of data and the parallel data is composed of N bits of data. Claim 31 depends from claim 30 and recites that N is equal to a predetermined number times M.

Claim 32 recites a method similar to claim 28 except that claim 32 recites a memory write method for writing data generated by a processor into a memory in accordance with a request from the processor. Claim 33 depends from claim 32 and recites that

the data received in parallel from the processor is composed of N bits of data. Claim 34 which depends from claim 32 recites that the M bits of data includes an M bit portion of N bits of data.

Claim 35 is directed to a data processing apparatus which includes memory means, data processing means, and memory control means for controlling transfer of data between the memory means and the data processing means. A first bus is provided having M lines interconnecting the memory means and the memory control means and a second bus having N lines interconnecting the data processing means and the memory control means wherein the memory control means includes converting means for converting M bits of data read out from the memory into N bits of data to be supplied in parallel to the data processing means. Claims 36 depends from claim 35 and recites that the M bits of data is successfully read out of the memory means in a time shared fashion plural times within a predetermined unit of time. Claim 37 depends from claim 36 and recites that the N bits of data converted from the M bits of data is applied to the data processing means in a unit of time more that two times the predetermined unit of time. Claim 38 depends from claim 35 and recites that the N bits of data includes M bit portions of the N bits of data. Claim 39 depends from claim 36 and recites that the M bits of data includes an N bit portion of N bits of data.

Claim 40 recites a memory control apparatus having interface means having M bit terminals coupled to a memory and N bit terminals coupled to data processing means. The interface means converts M bits of data from the memory means into N bits of data

to be supplied to the data processing means. Claim 41 depends from claim 40 and recites that the M bits of data includes a M bit portion of N bits of data.

Claim 42 is similar to claim 28 but recites that the converting step is performed by converting the successively read out data into parallel data by combining the successively read out data.

Claim 43 is directed to a memory controller for controlling transference of data between a memory and a processor similar to claim 40 except that claim 43 recites that M bit terminals are coupled to the memory, and N bit terminals are coupled to the processor. Converting means is provided for converting M bits of data into M bits of parallel data.

Claims 44-48 were added by way of an Amendment responding to the March 9, 1994 Office Action to further claim the board aspects of the invention erroneously not claimed in U.S. Patent No. 4,975,857. Particularly, claim 44 is directed to a graphic processing apparatus having a memory, a data processor, output means, a memory controller, a first bus having M bits and a second bus having N bits. The memory controller includes a storage for temporarily storing graphic data read out from the memory in a time shared fashion through the first bus, means for supplying the temporarily stored graphic data to the data processing means as N bits parallel data and a converter for converting the temporarily stored graphic data into serial data which is provided to the output means.

Claims 45-47 depend from claim 44 and claim 48 depends from claim 47. Claim 44 recites that the memory controller further includes a multiplexer for outputting the N bits graphic data transferred from the data processor to the first bus in a time shared fashion, claim 46 recites that the memory controller includes means for generating an address signal for accessing the memory plural times, in response to a signal for accessing the memory supplied from the data processor and claim 47 recites that the graphic data to be transferred to the memory controller through the first bus is read out from the memory plural times within a unit transfer time in a time shared fashion based on an access signal to the memory designated by the data processor.

Claim 48 recites that the graphic data transferred to the memory controller is supplied to the data processor through the second bus within a time longer than twice the unit transfer time.

The above-described deficiency in the original patent, U.S. Patent No. 4,975,857 arose without any deceptive intention on our part. More particularly, the error arose during the prosecution of U.S. Application Serial No. 302,332 filed January 27, 1989 from which U.S. Patent 4,975,857 issued due to our failure and that of our Japanese agent and U.S. attorneys to recognize as described above that the specification originally presented and amended by the Amendments filed on April 5, 1990 and September 10, 1990, disclosed a specific example of our invention as it relates to graphic processing apparatus and a more broader concept related to the transfer of data between a first bus and a

second bus wherein the size of the first bus is larger than the size of the second bus using a time sharing operation. The claims of U.S. Patent No. 4,975,857 were erroneously directed only to the specific example of our invention as it relates to graphic processing apparatus;

We hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Japanese Patent Application No. 63-93448, filed April 18, 1988, in Japan.

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

8/25/94 Koyo Katsura

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CONSENT OF ASSIGNEE

The undersigned assignee of the entire interest in the above-mentioned Letters Patent No. 4,975,857 hereby assent to the accompanying application.

HITACHI, LTD.

Sep. 14, 1994
Date

Katsuo OGAWA, Patent Attorney
General Manager, Patent Dept.